1. A method to produce a twin MONOS memory cell array, comprising:

a) preparing a semiconductor substrate to form cells of a twin MONOS memory array,

b) forming mask elements on a surface of said semiconductor substrate,

c) implanting a lightly doped region between said mask elements and within said lightly doped region implanting a heavily doped region,

d) forming a first insulator between said mask elements over said lightly doped region,

e) planarizing the surface of said substrate, and stopping when said mask elements are detected,

f) removing said mask elements and forming a second insulator over the surface of said substrate,

g) forming sidewall spacers on vertical edges of said second insulator between regions of said first insulator and removing exposed areas of said second insulator,

h) removing said sidewall spacers and forming a third insulator over surface of said substrate,

i) forming a conductive layer on said third insulator between said regions of the first insulator.

2. The method of claim 1, wherein preparing said semiconductor substrate further comprising:

a) forming shallow trench isolation in locations between columns of cells of said memory array,

b) growing a gate oxide of between about 2-5nm.

3. The method of claim 1 wherein said semiconductor substrate is a p-type substrate with a surface concentration of between about 5E17 and 1.5E18 atoms per cm^3.

4. The method of claim 1, wherein forming said mask elements further comprises:

a) depositing between about 100-250nm of polysilicon using CVD,

b) depositing on said polysilicon a nitride to a thickness between about 100-150nm,

c) patterning and etching said mask elements.

5. The method of claim 1, wherein implanting said lightly doped region is to a concentration of between about 3E12 and 3E13 atoms per cm^3.

6. The method of claim 5, wherein implanting said lightly doped region is at an energy level of between about 15-20keV.

7. The method of claim 1, wherein implanting said heavily doped region further comprises:

a) forming said sidewall spacers on said mask elements partially extending over said lightly doped region,

b) implanting said heavily doped region to a concentration of approximately about 1.5E15 atoms per cm^3.

8. The method of claim 7, wherein implanting said heavily doped region is at an energy level of 15-25keV.

9. The method of claim 1, wherein forming said first insulator between said mask elements is done by depositing an oxide using CVD to a thickness of between about 250-400nm.

10. The method of claim 1, wherein planarizing said surface of the substrate uses a chemical and mechanical polish stopping at a nitride layer of said mask elements.

11. The method of claim 1, wherein removing said mask elements further comprises:

a) removing an upper nitride layer using a selective etch,

b) removing a polysilicon layer using a selective etch using a dry chemical etch,

c) removing a gate isolation oxide formed during said preparation of said substrate,

d) growing a new gate oxide using a thermal process to a thickness of 2.5-5nm.

12. The method of claim 1, wherein forming a second insulator is done by depositing a nitride at a thickness of between about 6-9nm.

13. The method of claim 1, wherein forming said sidewall spacers is done with a disposable material which can be selectively etched against said first insulator comprising silicon oxide.

14. The method of claim 1 wherein forming said third insulator by ISSG (InSitu Steam Generation) further comprising:

a) growing an oxide on said second insulator to a thickness of approximately between 5-6nm,

b) growing said oxide on surface of substrate to a thickness of approximately between 8-12nm on said substrate where exposed areas of said second insulator were removed.

15. The method of claim 1, wherein forming a conductive layer further comprises:

a) depositing polysilicon by CVD to a thickness of approximately about 250nm,

b) polishing said polysilicon to planarize surface of said substrate using chemical mechanical polishing,

c) siliciding said polysilicon with Co or Ti.

16. A method to create cells for a twin MONOS memory array, comprising:

a) a means for depositing an array of N-type regions into a semiconductor substrate to define locations of cells for a twin MONOS memory,

b) a means for creating a first insulator over said N-type region in a defined shape,

c) a means for covering sidewalls of said first insulator with a thin layer of a second insulator wherein said second insulator extends partially into a space between two adjacent first insulators at a surface of said substrate forming an "L" like shape,

d) a means for forming a thin layer of a third insulator over said second insulator in said space,

e) a means for filling said space with a conductive layer covering said second and third insulators.

17. The method of claim 16, wherein said N-type region comprises a lightly doped region within which is a heavily doped region.

18. The method of claim 16, wherein said defined shape of said first insulator is created by CVD of an oxide between formed mask elements on the surface of said substrate and by removing said mask elements.

19. The method of claim 16, wherein said "L" like shape of said second insulator is formed by depositing a nitride on said first insulator, protecting said nitride with sidewalls covering said nitride on sides of said first insulator and etching exposed areas of said nitride.

20, The method of claim 19, wherein two adjacent feet of said "L" like shape of said nitride within said space forms two storage sites of said memory cell.

21. The method of claim 16, wherein said conductive layer is formed by a CVD of a polysilicon into said space between adjacent first insulators to create a word gate for said memory cell.

22. The method of claim 21, wherein said conductive layer extends across a row of said cells to form a word line for said memory.

23 The method of claim 17, wherein said N-type region connects between adjacent cells in a column.

23. A twin MONOS NAND memory array, comprising:

a) an array of twin MONOS memory cells arranged in rows and columns and forming a NAND memory array,

b) a word gate located over two storage sites of each memory cell of said memory cells,

c) a diffusion forming a source and a drain connecting between said memory cells in a column

d) a first selector gate located at top of a column and connected to a first memory cell in said column.

e) a second selector gate located at a bottom of a column and connected to a last memory cell in said column

24. The memory array of claim 23, wherein said word gate is a part of a word line, which is further a row of said word gates.

25. The memory array of claim 23, wherein said source and said drain are formed by a single diffusion located between adjacent memory cells in said column.

26. The memory array of claim 23, wherein said storage sites are nitride elements located below said word gate.

27. The memory array of claim 23, wherein said first and second selector gates select said column of memory cells to allow memory operations to be performed.

28. The memory array of claim 23, wherein said diffusions in rows are isolated from each other by a shallow trench isolation.

29. A NAND memory array using twin MONOS memory cells, comprising:

a) a means to locate two storage sites under each word gate of a twin MONOS memory array,

b) a means for connecting together said word gates in a row of said memory array,

c) a means for connecting together a plurality of memory cells in a column of said memory array, wherein said column has an upper voltage and lower voltage,

d) a means for selecting said upper voltage to be connected to said column,

e) a means for selecting said lower voltage to be connected to said column,

f) a means for performing memory operations by selecting said upper and lower voltages and by applying a plurality of voltages to the word gates of said plurality of cells in said column.

30. The memory array of claim 29, wherein said storage sites are nitride structures extending beneath said word gates.

31. The memory array of claim 29, wherein said means for connecting word gates together in a row is a word line deposited across said memory array and forming the word gates of each memory cell in said row.

32. The memory array of claim 29, wherein said means for connecting together said plurality of memory cells in a column is through a diffusion formed between each memory cell of said plurality of cells in said column.

33. A method for block erase of storage sites of a twin MONOS NAND memory array, comprising:

a) applying a high positive voltage to a selected word line,

b) applying a low voltage to unselected word lines,

c) applying a ground potential to a drain of an upper column selector gate,

e) applying a ground potential to a source of a lower column selector,

f) selecting said upper and lower column selectors and erasing both storage sites of each cell in a block of cells.

34. The method for block erase of claim 34, wherein said low voltage is of sufficient magnitude to allow the ground potential to be connected to a source and a drain of each cell in said block of cells through unselected cell in each column containing said block.

35. The method for block erase of claim 34, wherein erasing storage sites is an operation whereby electrons are injected into said storage sites by FN tunneling.

36. A method of programming storage sites in a twin MONOS NAND array, comprising:

a) selecting a first storage site to be programmed of two storage sites contained within a selected memory cell of a column memory cells,

b) connecting a negative voltage to a word gate of said selected memory cell,

c) connecting a positive voltage to a first diffusion extending under said first storage site,

d) connecting a ground potential to a second diffusion extending under a second storage site of said two storage sites,

e) programming said first storage site.

37. The method of programming of claim 37, wherein programming said first storage site is an operation whereby electrons are ejected from said first storage site by FN tunneling or hole injection.

38. The method of programming of claim 37, wherein connecting said positive voltage to said first diffusion further comprises:

a) connecting said positive voltage from a column selector gate by selecting said selector gate,

b) connecting a word line voltage higher in value than said positive voltage to unselected word gates in said column between said column selector gate and said first diffusion.

39. The method of programming of claim 37, wherein connecting said ground potential to said second diffusion further comprises:

a) connecting said ground potential from a column selector gate by selecting said selector gate,

b) connecting a word line voltage higher in value than said ground potential to unselected word gates in said column between said column selector gate and said second diffusion.

40. A method of reading storage sites in a twin MONOS NAND array, comprising:

a) selecting a first storage site to be read from two storage sites contained within a selected memory cell of a column memory cells,

b) connecting a first positive voltage to a word gate of said selected memory cell,

c) connecting a ground potential to a first diffusion extending under said first storage site to be read,

c) connecting a second positive voltage to a second diffusion extending under a second storage site not being read,

e) reading a current when the word gate voltage becomes higher than cell thresh hold voltage depending upon the data stored in said first storage site.

41. The method of reading storage sites of claim 41, wherein said first positive voltage is a value near a programmed threshold voltage of said memory cell.

42 The method of reading storage sites of claim 41, wherein said second positive voltage is less than said first positive voltage.

43 The method of reading storage sites of claim 41, wherein connecting said ground potential to said first diffusion further comprises:

a) selecting a column selector gate connecting said ground potential to said column,

b) applying a positive voltage to word lines of unselected memory cells between said column selector and said first diffusion.

44. The method of reading storage sites of claim 41, wherein connecting said second positive voltage to said second diffusion further comprises:

a) selecting a column selector gate connecting said second positive voltage to said column,

b) applying a positive voltage to word lines of unselected memory cells between said column selector and said second diffusion.

45. The method of reading storage sites of claim 41 further comprising:

a) said second positive voltage connected to said second diffusion produces a low threshold voltage for said second storage site,

b) said first storage site has a high threshold voltage when charged with electrons representing said first storage site not being programmed thereby blocking a flow of current,

c) said first storage site has said low threshold voltage when not charged with electrons representing said first storage site being programmed thereby allowing said flow of current,

d) said flow of current indicates a stored data value in said first storage site.

46. A second method to produce a twin MONOS memory cell array, comprising:

a) preparing a semiconductor substrate to form cells of a twin MONOS memory array,

b) forming mask elements on a surface of said semiconductor substrate,

c) implanting a lightly doped region between said mask elements and within said lightly doped region implanting a heavily doped region,

d) forming a first insulator between said mask elements over said lightly doped region,

e) planarizing the surface of said substrate, and stopping when said mask elements are detected,

f) removing said mask elements and forming a second insulator over the surface of said substrate,

g) forming a third insulator over the second insulator,

g) forming polysilicon sidewall spacers on vertical edges of said third insulator between regions of said first insulator and removing exposed areas of said third insulator and subsequently exposed second insulator and gate isolation insulator,

h) forming a fourth insulator over the exposed surface of the substrate and the sidewall spacers,

i) filling a first void between sidewall spacers and the fourth insulator with a polysilicon fill,

j) removing said polysilicon fill to approximately a half height from the surface of the substrate, creating a second void and exposing a portion of the fourth insulator,

k) Filling said second void with a metal connecting said polysilicon sidewalls with said polysilicon fill.

47. The method of claim 47, wherein preparing said semiconductor substrate further comprising:

a) forming shallow trench isolation in locations between columns of cells of said memory array,

b) growing a gate oxide of between about 2-5nm.

52. The method of claim 47 wherein said semiconductor substrate is a p-type substrate with a surface concentration of between about 5E17 and 1.5E18 atoms per cm^3.

53. The method of claim 47, wherein forming said mask elements further comprises:

a) depositing between about 100-250nm of polysilicon using CVD,

b) depositing on said polysilicon a nitride to a thickness between about 100-150nm,

c) patterning and etching said mask elements.

54. The method of claim 47, wherein implanting said lightly doped region is to a concentration of between about 3E12 and 3E13 atoms per cm^3.

55. The method of claim 51, wherein implanting said lightly doped region is at an energy level of between about 15-20keV.

56. The method of claim 47, wherein implanting said heavily doped region further comprises:

a) forming said sidewall spacers on said mask elements partially extending over said lightly doped region,

b) implanting said heavily doped region to a concentration of approximately about 1.5E15 atoms per cm^3.

48. The method of claim 53, wherein implanting said heavily doped region is at an energy level of 15-25keV.

49. The method of claim 47, wherein forming said first insulator between said mask elements is done by depositing an oxide using CVD to a thickness of between about 250-400nm.

50 The method of claim 47, wherein planarizing said surface of the substrate uses a chemical and mechanical polish stopping at a nitride layer of said mask elements.

51. The method of claim 47, wherein removing said mask elements further comprises:

a) removing an upper nitride layer using a selective etch,

b) removing a polysilicon layer using a selective etch using a dry chemical etch,

c) removing a gate isolation oxide formed during said preparation of said substrate,

d) growing a new gate oxide using a thermal process to a thickness of 2.5-5nm.

57 The method of claim 47, wherein forming said third insulator over the second insulator is to a thickness of in a range of approximately 4nm-7nm using a CVD process.

58 The method of claim 47, wherein forming said fourth insulator to a thickness in a range approximately between 2.5nm and 6nm.

59. The method of claim 47, wherein filling said second void with said metal comprises a barrier metal.

60. The method of claim 60, wherein said barrier metal is titanium nitride.

61. The method of claim 60, wherein said barrier metal is titanium.